

APPLICATION

FOR

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TITLE: POWER GRIDDING SCHEME

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POWER GRIDDING SCHEME

BACKGROUND

The invention generally relates to a power gridding scheme.

Microprocessors are being fabricated with increasingly higher speeds and device density.

5 As a result, the power that is consumed by a microprocessor continues to increase from one generation to the next. This increase in power usage, in turn, may present several challenges.

For example, the microprocessor has a finite number of external contacts (positive and negative supply voltage contacts, for example) to communicate power to the microprocessor. For example, these external contacts may be solder bumps that are part of a ball and grid package, a package in which the solder bumps are arranged in a rectangular grid, or array. In this array, the distances between adjacent solder bumps typically decreases from one generation microprocessor to the next in an attempt to increase the number of solder bumps that are available to communicate power. However, the increase in bump density does not track the corresponding increase in the speed and scaling of devices in the microprocessor. As a result, there is a net reduction in the number of solder bumps for power per device in the microprocessor. Thus, the net result of the increased power density for these solder bumps is that the current densities of some solder bumps may be large enough to possibly cause premature failure of these solder bumps due to the process of electromigration (EM).

Thus, there is a continuing need for an arrangement that addresses one or more of the
20 problems that are stated above.

BRIEF DESCRIPTION OF THE DRAWING

Fig. 1 is a partial schematic diagram of an integrated circuit package depicting an arrangement of solder bumps according to an embodiment of the invention.

Fig. 2 is a cross-sectional view of the package taken along line 2-2 of Fig. 1.

25 Fig. 3 is an exploded perspective view of a portion of the package according to an embodiment of the invention.

Fig. 4 is a top view of an interconnection layer of Fig. 3 according to an embodiment of the invention.

Fig. 5 is a cross-sectional view of a semiconductor package according to an embodiment of the invention.

Fig. 6 is a top view of an integrated circuit die according to an embodiment of the invention.

5 Fig. 7 is a schematic diagram depicting electrical connections between buses and solder bumps according to an embodiment of the invention.

Figs. 8, 9 and 10 are exploded perspective views of portions of semiconductor packages according to different embodiments of the invention.

10 Fig. 11 is a cross-sectional view of a portion of a semiconductor package according to an embodiment of the invention.

DETAILED DESCRIPTION

15 Referring to Fig. 1, an integrated circuit package (a microprocessor, as an example) in accordance with an embodiment of the invention includes solder bumps 22 that are located on the outside of the package 10 to form external contacts. In this manner, the package 10 may be a ball grid package, and the solder bumps 22 may be part of a grid, or array. The solder bumps 22 form contacts for communicating power and signals to and from circuitry of the integrated circuit package 10. As an example, some of the solder bumps 22 may be designated to communicate positive and negative supply voltages to the integrated circuit package 10.

20 More particularly, Fig. 1 depicts, as examples, specific solder bumps 22a, 22b and 22c (for example) that may be used to communicate power to various circuitry of the integrated circuit package 10. For this example, the solder bumps 22a, 22b and 22c may all communicate the same positive power supply voltage. The solder bumps 22a, 22b and 22c may be electrically connected to different internal power, or supply voltage, buses 17 of the integrated circuit package 10. In this manner, the solder bumps 22a and 22b may be electrically connected to one
25 positive supply voltage bus 17a of the integrated circuit package 10, and the solder bump 22c may be electrically connected to another positive supply voltage bus 17b of the integrated circuit package 10.

30 Although the positive supply voltage buses 17 are described below in connection with the solder bumps 22a, 22b, and 22c, it is understood that the same principles apply for other supply voltage buses, such as a negative supply voltage bus 18, for example.

To establish both an electrical and mechanical connection between a particular solder bump 22 and circuitry inside the integrated circuit package 10, a window may be formed in a passivation layer of the semiconductor die that is encased in the package 10. This passivation layer forms an outer insulating layer of the die 11 and is located between the closest internal metal layer of the package 10 and the solder bumps 22. As a more specific example, referring also to Fig. 2, the integrated circuit package 10 may include a passivation layer 16 that generally covers an upper metal layer 62 (a metal six layer, as an example) of the die 11. The metal layer 62 is exposed for contact with the solder bumps 22 at several locations at which contact windows are formed in the passivation layer 16.

One of these windows 15 is depicted in Fig. 2. As shown, the window 15 exposes a solder bump metal contact pad 66 that is part of the upper metal layer 62. Thus, the associated solder bump 22a extends through the window 15 to bond to the metal pad 66. This metal pad 66, in turn, is electrically connected to the supply voltage bus 17a, and thus, the contact of the solder bump 22a to the metal pad 66 electrically connects the solder bump 22a to the bus 17a. As an example of the interconnection between the metal pad 66 and the bus 17a, the pad 66 may be connected to a metal pad 70 of a lower metal layer 64 by way of a via 67, and this metal pad 70 may be connected to the bus 17 by way of another via 71.

The size of the window 15 limits the current carrying capability of the solder bump 22, as the size of the window 15 defines the area of the solder bump 22 that contacts the solder bump contact pad 66. For purposes of increasing the extent of contact between the solder bump 22 and the contact pad 66, in accordance with an embodiment of the invention, the window 15 is elongated. This elongation permits more contact area between solder bump 22 and its associated contact pad 66. Thus, selected windows of the integrated circuit package 10 may be elongated for purposes of increasing the current carrying capabilities of solder bumps 22 that communicate positive and negative supply voltages.

As a more specific example, referring back to Fig. 1, in some embodiments of the invention, the window 15 may be a substantially rectangular pad, a pad that is elongated such that the longest dimension of the window 15 is aligned with the bus 17 that lies underneath that window 15 and is electrically connected to the solder bump 22 that extends through the window 15. Thus, the major axis of the rectangular window 15 is aligned with and located directly above the bus 17 that extends immediately below the window 15.

In contrast to the elongated shape of the window 15, a window 14 of the prior art, also depicted in Fig. 1 for purposes of comparison, typically is square. In this manner, in conventional integrated circuits, the size of the square window is limited by the dimension (of the square window 14) that is transverse to the bus 17. In contrast, unlike conventional arrangements, in the integrated circuit 10, although the transverse direction governs the width of the window 15, the length of the window 15 is elongated along the bus 17 in a direction to permit more contact between the associated solder bump 22 and contact pad 66.

As a more specific example, in some embodiments of the invention, the window 15 may have a dimension of approximately 80 by 40 micrometers (μm , or microns), and in other embodiments of the invention may have dimensions of 100 by 150 microns.

It is noted that it is not essential that the window 15 has a rectangular shape. In this manner, in other embodiments of the invention, the window 15 may have different elongated shapes (an oval shape, for example).

As depicted in Fig. 1, in some embodiments of the invention, the windows that are formed in the passivation layer 16 are sized differently. In this manner, the windows, in some embodiments of the invention, are selectively sized, in that larger windows are formed for use with some solder bumps 22 and smaller windows are formed for use with other solder bumps 22. Such an arrangement permits larger windows to be formed for solder bumps 22 that carry relatively high levels of currents, thereby increasing the current carrying capabilities of these solder bumps 22; and permits smaller windows to be formed for solder bumps 22 that do not carry such high levels of current.

As an example of this selective sizing, Fig. 1 depicts the rectangular windows 15 that are relatively large and are used to increase the current carrying capabilities of solder bumps 22a and 22b, as compared to hexagonal windows 11 that are used by solder bumps 22d and 22e. The hexagonal window 11 is smaller than the window 15 in that the window 11 exposes less area of the upper metal layer for contact with the associated solder bump 22 than the window 15. Thus, the solder bumps 22d and 22e may be associated with lower currents than the solder bumps 22a and 22b, for example, and the sizes of their associated windows reflect this lower current load.

In some embodiments of the invention, as an example of this selective sizing, some of the windows may be approximately square and have dimensions of approximately 40 by 40 microns; and other larger windows (sized to impart a higher current capability to their associated solder

bumps 22) may have dimensions of approximately 80 by 40 microns. As another example, in other embodiments of the invention, some of the windows may be approximately square and have dimensions of approximately 100 by 100 microns; and other larger windows (sized to impart a higher current capability to their associated solder bumps 22) may have dimensions of approximately 100 by 150 microns. Other variations, size differences and shapes of the windows are contemplated and are within the scope of the appended claims.

Fig. 3 depicts another embodiment 200 for the integrated circuit package. In this embodiment, the package 10 includes different features to increase the current carrying capability of the solder bumps 22. In this arrangement, the integrated circuit 10 includes an interconnection layer 26 to establish separate and redundant connections between the solder bumps 22 and the buses 17. For example, in some embodiments of the invention, the interconnection layer 26 may form bridges (such as bridges that form a triangle 30, as more clearly depicted in a top view in Fig. 4) that form redundant connection points 23 between the solder bumps 22a, 22b and 22c. As depicted in Fig. 3, these bridges may be part of a metal layer that is located between the solder bumps 22 and a metal layer in which the buses 17 are formed. However, in other embodiments of the invention, the interconnection layer 26 may be formed out of the same metal layer as the buses 17.

Fig. 5 depicts a cross-sectional view of the integrated circuit 200, depicting the interconnection layer 26 as being part of the upper metal layer 62. More particularly, Fig. 5 depicts a portion 208 of the metal layer 62 that forms redundant connections between solder bumps 22 (two solder bumps 22 being depicted in Fig. 5). In this manner, each solder bump 22 is also connected to the bus 17 that is formed in the lower level metal layer 65. The integrated circuit 200 may have additional metal layers that are disposed between the metal layers 62 and 65, such as a metal layer 64 that is depicted in Fig. 5. In this manner, the metal layer 64 may include metal pads 212 that are connected to the metal portion 208 through vias 210, and the metal pads 212 may be connected to the bus 17 through other vias 214.

Referring to Fig. 7, the electrical path between a solder bump 22 for a supply voltage and the corresponding bus 17 may be electrically represented by a resistor 100. However, unlike conditional arrangements, the interconnection layer 26 forms redundant connections (depicted by the electrical connections 102 between the solder bumps 22), thereby effectively shorting the

solder bumps 22 together near the top of the die to form a lower resistance between each solder bump 22 and its associated bus 17.

Although the interconnection layer 26 has been described above in connection with an integrated circuit package that includes solder bumps 22, other arrangements are possible. For example, Fig. 6 depicts a top surface of a die 40 that includes bond pads 44 for communicating supply voltage to and from the die 40. The interconnection layer may be formed, for example, by metal lines 50, or bonding wire, that connects various bond pads 44 together. For example, the bond pads denoted by the reference numeral "44b" are connected together via the conductive traces 50. Other arrangements are possible.

Fig. 8 depicts an integrated circuit package 400 in which the interconnection layer 26 is formed from conductive traces 150, 152 and 154, all of which lie in the same metal layer. Vertical vias 160 form connections between the traces 150, 152 and 154 and the associated buses 17.

Fig. 9 depicts an integrated circuit package 450 in which the interconnection layer 26 is formed in the same metal layer as the buses 17. For example, in some embodiments of the invention, the interconnection layer 26 may be formed by a conductive trace 120 that connects two of the buses 17 together, and another conductive trace 122 that connects the other bus 17 to the two connected buses. Other arrangements are possible.

Fig. 10 depicts another integrated circuit package 500. In the package 500, the interconnection layer 26 contains circuitry other than hard-wired conductive traces. In this manner, in some embodiments of the invention, the interconnection layer 26 may include switches, such as metal-oxide-semiconductor field-effect-transistors (MOSFETs) 500, that have their drain-source paths coupled between various solder bumps 22 to selectively form connection points 23 near the solder bumps 22. Thus, due to this arrangement, the MOSFETs 500 may be selectively closed to couple groups of the solder bumps 22 together. This arrangement may have various advantages, such as permitting grouping of the solder bumps 22 after fabrication of a particular integrated circuit. In this manner, it may be determined that certain solder bumps 22 require higher current densities than other solder bumps 22. Thus, the solder bumps 22 that require higher densities are connected together to effectively impart a higher current carrying capability to each of these bumps 22.

Other embodiments are within the scope of the following claims. For example, Fig. 11 depicts an arrangement in which an extra metal layer 533 (a metal seven layer, for example) is created on top of the passivation layer 16 (i.e., on the opposite side of the passivation layer 16 from the other metal layers) for purposes of forming part or all of the interconnection layer 26.

5 In this manner, the metal for the metal layer 533 may be deposited on top of the passivation layer 16. Next, a mask is used to form an etching pattern for purposes of permitting subsequent etching to remove metal from the metal layer 533 while leaving conductive traces (the trace 534 depicted in Fig. 11, as an example) to selectively form connections between the solder bumps 22. As depicted in Fig. 11, in an example, two solder bumps 22f and 22g are connected together by a
10 conductive trace 534 of the metal layer 533. The solder bumps 22f and 22g extend through respective windows to contact respective metal pads 540 of the next lower metal layer 62. Other variations are possible.

15 While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.